REMARKS

The present response is to the Office Action mailed in the above-referenced case on October 29, 2003, made final. Claims 1-42 are pending for examination. Claims 1-3, 5-6, 8-12, 15-17, 19-20, 22-26, 29-31, 33-34 and 36-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Nemirovsky (DISC, A Dynamic Stream Computer), hereinafter Nemirovsky.

Claims 4, 13-14, 18, 27-28, 32 and 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nemirovsky as applied to claims 1-3, 5-6, 8-12, 15-17, 19-20, 22-26, 29-31, 33-34 and 36-40, and further in view of Nemirovsky et al. (DISC, A Dynamic Stream Computer), hereinafter Nemirovsky et al. Claims 7, 21 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nemirovsky as applied to claims 1-3, 5-6, 8-12, 15-17, 19-20, 22-26, 29-31, 33-34 and 36-40, and further in view of applicant's admission.

Applicant has again carefully studied the prior art presented by the Examiner, and the Examiner's rejections and statements in the instant Office Action. In response, applicant herein presents further argument to more particularly point out the key and patentable distinction of applicant's invention as recited in the base claims and to establish that the claims clearly and unarguably patentable over the prior art reference.

Applicant herein addresses the Examiner's "Response to Arguments" section of the current Office Action. Applicant previously put forth the argument that the prior art of Nemirovsky fails to teach a plurality of physical hardware streams for streaming one or more instruction threads.

The Examiner responds to the argument stating the DISC concept as taught by Nemirovsky relies on a structure maintaining several simultaneous instructions which are dynamically controlled by the processor (see page 63, 69). In addition, the Examiner continues, the instruction interleaving with several

simultaneous instructions allows the DISC to obtain high instruction throughput which is impossible to achieve in a conventional architecture.

Applicant argues the DISC computing system of Nemirovsky is extremely limited by the "pipeline" type instruction stream layering which makes it virtually impossible for instruction streams to truly simultaneously process instruction. Nemirovsky teaches a DISC (page 36). As explained in Nemirovsky, an important feature of DISC is that the instruction stream partition dynamically changes to optimize the processor utilization. Applicant points out that DISC utilizes pipelining in which multiple instructions **from a (that is...one) sequential instruction stream** are simultaneously executed in an overlapped faction.

Nemirovsky teaches that a pipeline is compared to an assembly line in that the instruction is divided into multiple steps, the steps are called pipe stages. The stages are connected in a line, one next to the other, to form a pipe. Then an instruction is introduced at every single cycle at one end of the pipe while another exits the pipeline at the other end. Nemirovsky teaches that each stage of the pipeline processes a different piece of instruction simultaneously.

Applicant agues that this pipeline system is one instruction stream divided into 4 separate sub-streams segmented into steps in a pipeline. Surely the Examiner can understand how this pipeline system fails to read on a plurality of physical hardware streams in a multi-steaming processor, as claimed.

The background portion of applicant's specification defines a *stream* in reference to a processing system as a *hardware* capability of the processor for supporting and processing an instruction thread. The maximum capability of any multi-streaming processor to process multiple concurrent *threads* remains fixed at the number of hardware *streams* the processor supports. Clearly, Nemirovsky's DISC is a single hardware stream partitioned and fails to anticipate a true multi-stream processor as claimed.

Applicant further argues that the type of pipeline for an instruction stream as disclosed could not accommodate a flexible, dynamic mapping of interrupts

and streams as claimed. As shown in Fig. 5.12, showing the sequencer of DISC architecture, streams and interrupts are assigned prior to streams actually detecting any interrupts. Clearly, Nemirovsky teaches away from applicant's invention as claimed.

Applicant believes claims 1, 15 and 29 are patentable over the art of Nemirovsky. Claims 2-14, 16-28 and 30-42 are patentable o their own merits, or at least as depended from a patentable claim.

Applicant further argues the Examiner's rejection to claims 7, 21 and 35, specifically. The Examiner relies on Applicant's own admission, as interpreted in applicant's argument provided in response to a rejection presented by the Examiner. The said portion of applicant' argument from paper No. 8 is reproduced as follows:

"Regarding the Examiner's 112 rejection of applicant's claims 7, 21, and 35, the Examiner stated that the claims contain subject matter which was not adequately described in the specification, and that applicant has merely supplied a suggestion to do. In the previous response applicant respectfully pointed out to the Examiner that conditional and dynamic mapping, as recited in the claims, is but one of several possible mechanisms used for processing external interrupts once an external interrupt has been detected. The interrupt logic receives the interrupt and decides which stream or streams to interrupt depending on the type of interrupt and on one or any combination of said mechanisms.

Applicant is perplexed by the Examiner's insistence that further detail be given for conditional and dynamic mapping, which is but one of several such known mechanisms described in applicant's specification. For example, static mapping of interrupts, and programmable mapping of interrupts and exceptions are two other well-known mapping mechanisms which are described in applicant's specification, and are also recited in applicant's claims."

Clearly, applicant makes no such statement that dynamic mapping is well known in the art. Applicant only refers to dynamic mapping as known in applicant's specification. Further, applicant believes that if the Examiner were to

accurately use "Applicant's own admission" as an aid in a rejection it should come directly from applicant's specification, not an argument in a Response provided by applicant. Therefore, the Examiner's rejection of claims 7, 21 and 35 is certainly in error.

As all of the claims standing for examination as amended have been shown to be patentable over the art of record, applicant respectfully requests reconsideration and that the present case be passed quickly to issue. If there are any time extensions needed beyond any extension specifically requested with this amendment, such extension of time is hereby requested. If there are any fees due beyond any fees paid with this amendment, authorization is given to deduct such fees from deposit account 50-0534.

Respectfully Submitted
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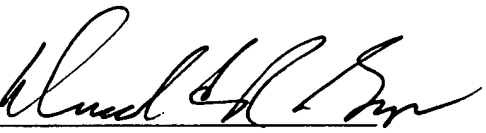
by 
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